Reg. No. : ☐☐☐☐☐☐☐☐☐☐☐☐☐

Question Paper Code : 80346

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Sixth Semester

Medical Electronics

EC 6601 — VLSI DESIGN

(Common to Electronics and Communication Engineering and also Common to Seventh Semester for Biomedical Engineering Electronics and Instrumentation Engineering and Robotics and Automation Engineering)

(Regulations 2013)
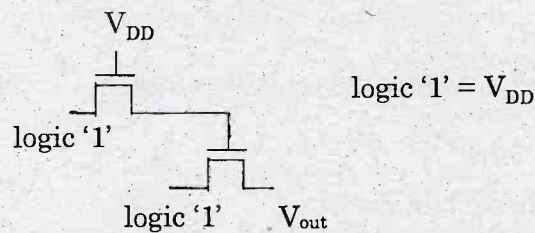
Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define body bias effect.

2. Draw the stick diagram and layout for CMOS inverter.

3. What is the value of V_{out} for the figure shown below, where V_{tn} is threshold voltage of transistor?

logic '1' = V_{DD}

4. List out the sources of static and dynamic power consumption.

5. What is meant by pipelining?

6. Draw the schematic of dynamic edge-triggered register.

7. Why is barrel shifter very useful in the designing of arithmetic circuits?

8. Write the principle of any one fast multiplier?

9. What is the standard cell-based ASIC design?

10. What is an antifuse? State its merits and demerits.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. (12)

   (ii) Derive the noise margins for a CMOS inverter. (4)

Or

(b) (i) Discuss in detail with a neat layout, the design rules for a CMOS inverter. (8)

    (ii) Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors. (8)

12. (a) Write short notes on :

    (i) Ratioed Circuits (8)

    (ii) Dynamic CMOS Circuits. (8)

Or

(b) (i) Estimate least delay and determine input capacitance of each stages for the logic network shown in figure, which may represent the critical path of a more complex logic block. The output of the network is loaded with a capacitance which is 5 times larger than the input capacitance of the first gate, which is a minimum-sized inverter. (8)
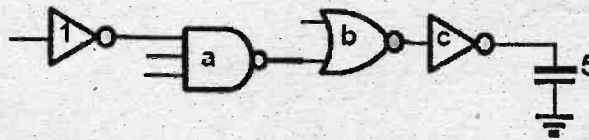
    (ii) Explain the dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. (8)

13. (a) Discuss in detail various static latches and registers. (16)

Or

(b) Write short notes on :

    (i) True single-phase clocked register (8)

    (ii) NORA – CMOS latches. (8)

14. (a) Explain the operation of a basic 4 bit adder, Describe the different approaches of improving the speed of the adder. (16)

Or

(b) Explain the operation of booth multiplication with suitable examples? Justify how booths algorithm speed up the multiplication process. (16)

15. (a) Discuss the different types of programming technology used in FPGA design. (16)

Or

(b) Briefly explain the semi custom ASIC with its classification. (16)

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